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TRANSMITTAL FORM

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Total Number of Pages in This Submission	47

Application Number	09/648,173
Filing Date	08/25/2000
First Named Inventor	Rajeev JAYAVANT, et al.
Art Unit	2676
Examiner Name	SINGH, Dalip K.
Attorney Docket Number	1458-P04211

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
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SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	TOLER, LARSON & ABEL, LLP		
Signature			
Printed name	Paul J. Polansky		
Date	May 2, 2005	Reg. No.	33,992

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PTO/SB/17 (12-04)
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Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT	($) 500.00

Complete if Known	
Application Number	09/648,173
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METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 01-0365 Deposit Account Name: Advanced Micro Devices, Inc.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

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FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

	FILING FEES		SEARCH FEES		EXAMINATION FEES		
		Small Entity		Small Entity		Small Entity	
Application Type	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	
Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round **up** to a whole number) x	_____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: Filing of a Brief in Support of an Appeal	500.00

SUBMITTED BY

Signature	Paul J. Polansky	Registration No. (Attorney/Agent) 33,992	Telephone 512-327-5515
Name (Print/Type)	Paul J. Polansky		Date 5/2/05

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Rajeev JAYAVANT et al.

For: CIRCUITRY AND SYSTEMS FOR PERFORMING TWO-DIMENSIONAL MOTION COMPENSATION USING A THREE-DIMENSIONAL PIPELINE AND METHOD OF OPERATING THE SAME

App. No.:	09/648,173	Filed:	August 25, 2000
Examiner:	Dalip K. SINGH	Group Art Unit:	2676
Customer No.:	34456	Confirmation No.:	6232
Atty. Dkt. No.:	1458-P04211		

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BRIEF IN SUPPORT OF APPEAL

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This brief contains these items under the following headings, and in the order set forth below (37 C.F.R. § 41.37(c)(1)):

TABLE OF CONTENTS

The final page of this brief before the beginning of the Appendix of Claims bears the attorney's signature.

I. REAL PARTY IN INTEREST (37 C.F.R. § 41.37(c)(1)(i))

The real party in interest in this appeal is Advanced Micro Devices, Inc., the assignee, as evidenced by the assignment recorded at Reel 015325, Frame 0168.

II. RELATED APPEALS AND INTERFERENCES (37 C.F.R. § 41.37(c)(1)(ii))

There are no interferences or other appeals that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS (37 C.F.R. § 41.37(c)(1)(iii))

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

There are thirty (30) claims pending in the application (claims 1-30).

B. STATUS OF ALL THE CLAIMS

1. Claims pending:

   Claims 1-30.

2. Claims withdrawn from consideration but not canceled:

   NONE.

3. Claims allowed:

   NONE.

4. Claims objected to:

   NONE.

5. Claims rejected:

   Claims 1-30 are rejected under 35 U.S.C. § 103(a).

6. Claims canceled:

NONE

C. CLAIMS ON APPEAL

There are thirty (30) claims on appeal, claims 1-30.

IV. STATUS OF AMENDMENTS (37 C.F.R. § 41.37(c)(1)(iv))

Amendments to claims 1, 7-13, 20-23 and 25 to correct various informalities and to remove reference to "step for" language were submitted subsequent to the final office action dated October 4, 2004 (hereinafter, "the Final Rejection"). The advisory action dated February 11, 2005 (hereinafter, "the Advisory Action") failed to indicate whether the amendments were entered. As the amendments are not material to the scope of the claims, it is believed that the amendments were entered or should have been entered. The remarks herein therefore are provided based on the assumption that the amendments were entered. However, the merits of the statements made herein are in no way reliant on or relevant to the amendments.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER (37 C.F.R. § 41.37(c)(1)(v))

The following summary is provided to give the Board the ability to quickly determine where the claimed subject matter appealed herein is described in the present application and is not to limit the scope of the claimed invention.

Independent claim 1 recites the features of image processing circuitry, comprising: a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space; a three-dimensional image pipeline

having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space; and dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

Independent claim 7 recites the features of: for use in image processing circuitry that comprises a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating dual mode sub-processing circuitry that is associated with both of said pipelines, said method comprising: determining whether said dual-mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; performing motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said two-dimensional mode; and performing rasterization operations associated said three-

dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said three-dimensional mode.

Independent claim 14 recites the features of: mode control circuitry for use in an image processing system having a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that processes two dimensional image data to generate successive two-dimensional image frames and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames, said mode control circuitry comprising: dual mode sub-processing circuitry, associated with each of said two-dimensional and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof; and a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in said two-dimensional mode and to perform said rasterization operations in said three-dimensional mode.

Independent claim 20 recites the features of: for use in image processing circuitry that comprises a two- dimensional image pipeline having a plurality of stages including a first stage and a last stage and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a

two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating mode control circuitry that is associated with both of said pipelines, said method comprising: determining whether dual mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; and controlling said dual mode sub-processing circuitry to perform either motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof in said two-dimensional mode, or rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof in said three-dimensional mode.

Independent claim 26 recites the features of: a media processing system having a central processing unit, a memory subsystem, an image processing system, and a display system, said media processing system comprising: a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space of said display system; a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space of said display system; and dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing

circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

Independent claim 27 recites the features of processing apparatus comprising: a first specialty pipeline having a plurality of stages including a first stage and a last stage; a second specialty pipeline having a plurality of stages including a first stage and a last stage; and dual mode sub-processing circuitry operable in a selected one of first and second modes wherein in said first mode said dual-mode sub-processing circuitry forms an intermediate stage of said first specialty pipeline and in said second mode said dual-mode sub-processing circuitry forms an intermediate stage of said second specialty pipeline.

Figures 1, 3, 4 and 5 of the present application and their corresponding disclosure are illustrative of an exemplary embodiment of the subject matter of independent claims 1, 7, 14, 20, 26 and 27. Figure 1 (reproduced below) illustrates an image processing system 115 including "circuitry for (i) a two-dimensional image pipeline 130 which is operable to process two-dimensional image data to generate successive two-dimensional image frames, and (ii) a three-dimensional image pipeline 135, which is operable to process three-dimensional image data to render successive three-dimensional image frames. . . ." Present Application, p. 13, lines 11-17. Image processing system 115 further includes dual-mode sub-processing circuitry 140 that is "operable to perform (i) motion compensation operations associated with two-dimensional image pipeline 130 in one mode, and (ii) rasterization operations associated [with] three-dimensional image pipeline 135 in another mode. Exemplary dual-mode sub-processing circuitry 140 advantageously employs the inherent symmetries of the functional units performing the motion compensation operations in two-dimensional pipeline 130 on the one hand and the rasterization operations in three-dimensional pipeline 135 on the other hand" Id., p. 13, line 21 – p. 14, line 7.

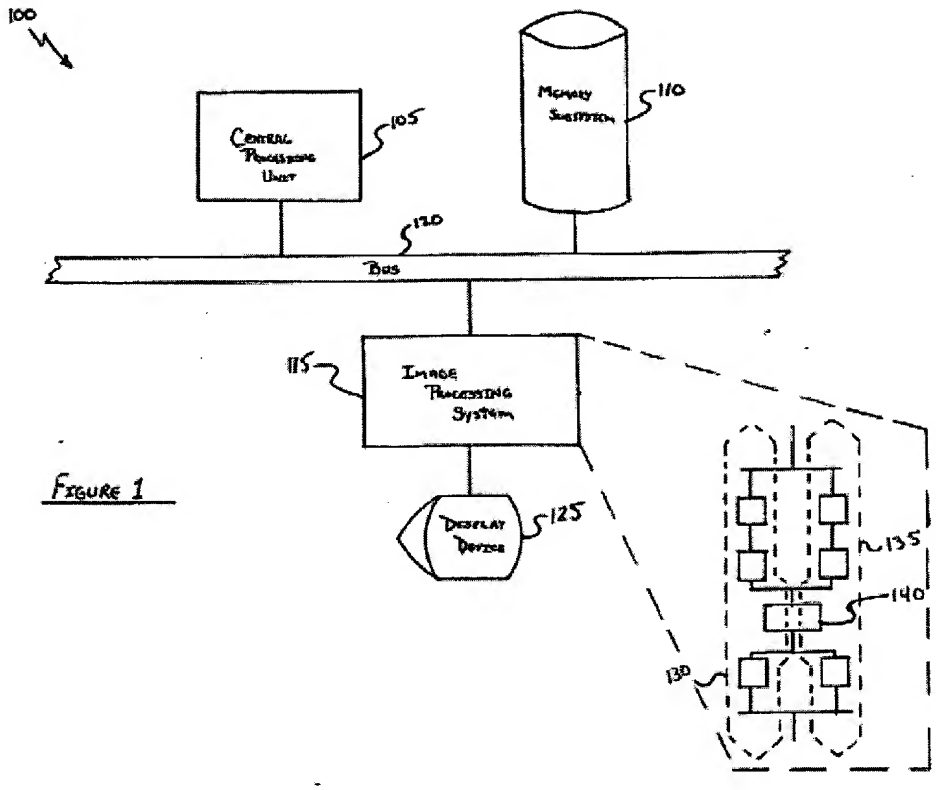


FIGURE 1

The Present Application, Figure 1

Figure 3 (reproduced below) of the present application illustrates an exemplary implementation of the image processing system 115. As depicted, the image processing system 115 includes a host interface 250, image processing circuitry 255 and a display controller 260. The image processing circuitry 255 includes a three-dimensional rasterizer 300, a setup controller 305, a VGA 310 and an arbiter 315. The rasterizer 300, in one embodiment, "is operable to perform common three-dimensional rasterization operations including processing triangles, vectors, planar trapezoids, alpha blending, and the like, as well as to perform texture mapping operations when image processing system 115 is in three-dimensional mode, and to perform two-dimensional motion compensation operations associated with the two-dimensional image pipeline when image processing system 115 is in two-dimensional mode." See Id., p. 18, line 19 – p. 19, line 7.

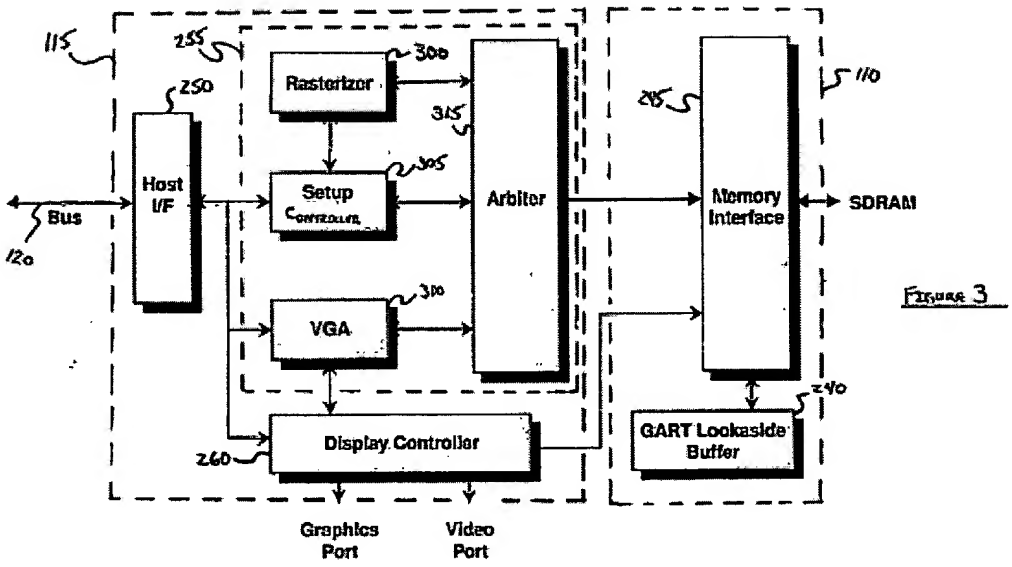


Figure 3

The Present Application, Figure 3

Figure 4 (reproduced below) of the present application illustrates an exemplary embodiment of the rasterizer 300. As provided by the present application, exemplary dual-mode sub-processing circuitry of the rasterizer 300 may include lighting/mixture blend circuitry 445, alpha blend circuitry 455, format/dither circuitry 460, U/V/Q interpolator 465, address generation circuitry 475, texture cache circuitry 480, format/filter circuitry 485, "8x8" pattern circuitry 490, mono expansion circuitry 495, and raster operation circuitry 499. See Id., p. 24, lines 4-8. These circuitry components are operable "to perform rasterization operations associated [with] said three-dimensional image pipeline in a default mode and to perform motion compensation operations associated with the two-dimensional image pipeline in the other mode." See Id., p. 24, lines 9-13. The present application further discloses how the components of the dual-mode sub-processing circuitry may perform either 2-D or 3-D operations depending on mode. See Id., p. 24, line 14 – p. 28, line 3. To illustrate, the lighting/mixture blend circuitry 445 "operates to combine multiple textures and the color from ARGB interpolator 440 using a variety of multiply/add operations" while in 3-D image processing mode, and "operates to

combine multiple reference frames by averaging" when in two-dimensional image processing mode. See Id., p. 24, lines 14 - 22.

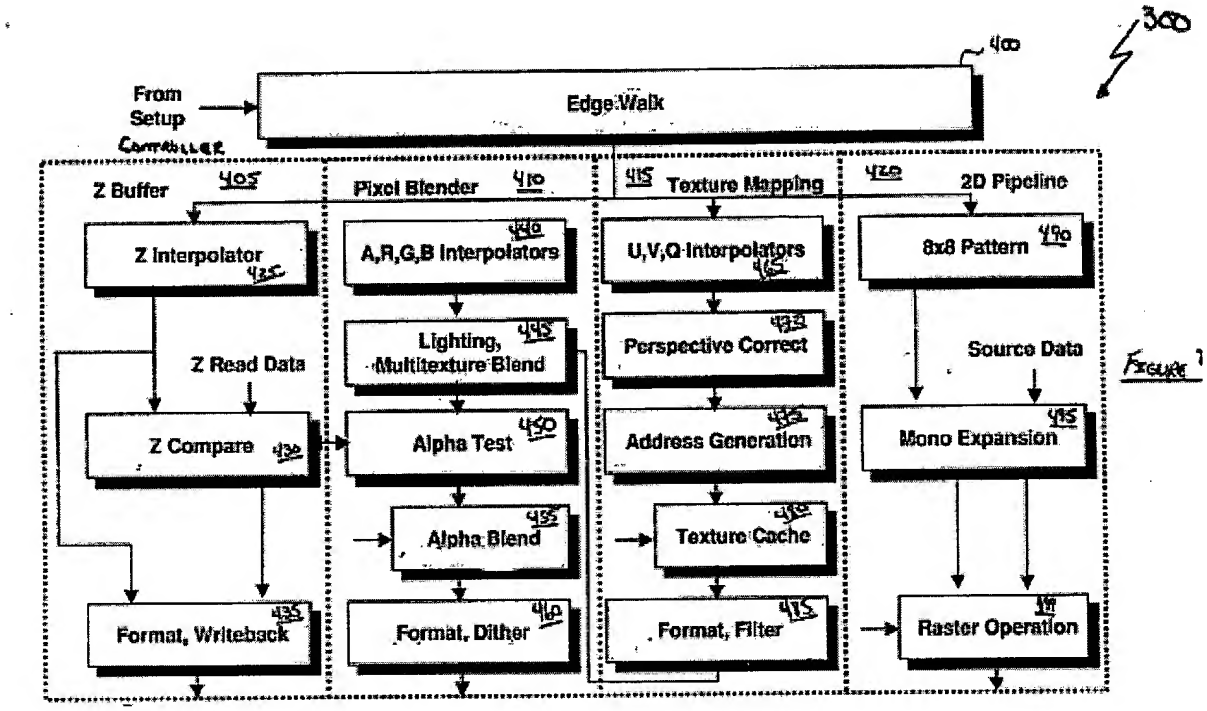
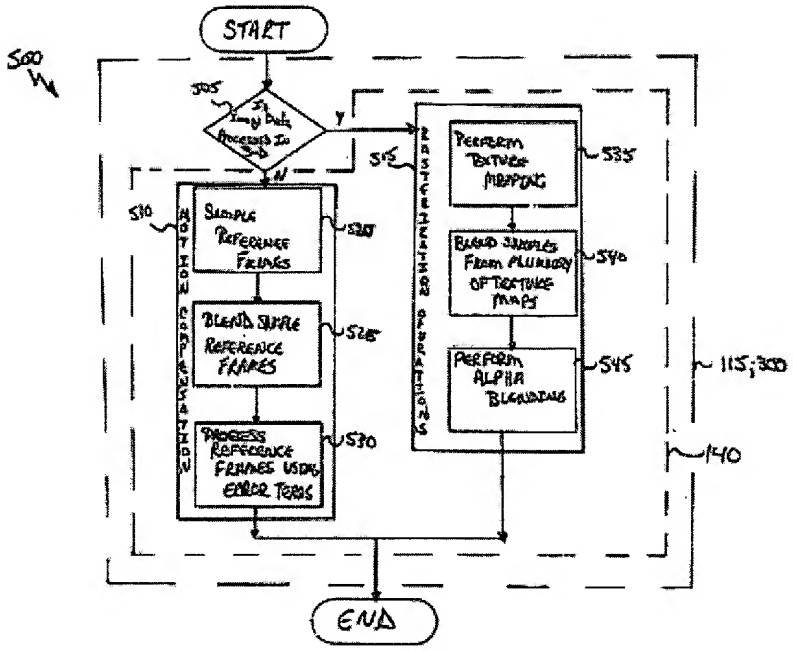


Figure 1

The Present Application, Figure 4

Figure 5 (reproduced below) and its related disclosure in the present application describe an exemplary method of operating the image processing system having the rasterizer 300 so that the dual-mode sub-processing circuitry 140 may be utilized by both the two-dimensional pipeline 130 and the three-dimensional pipeline 135.



The Present Application, Figure 5

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL (37 C.F.R. § 41.37(c)(1)(vi))

Claims 1-30 are rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent No. 5,394,524 to DiNicola *et al.* (hereinafter, "the DiNicola reference") in view of U.S. Patent No. 6,275,329 to Ezer *et al.* (hereinafter, "the Ezer reference") and further in view of U.S. Patent No. 6,208, 350 to Herrera (hereinafter, "the Herrera reference") as set forth in the Final Rejection.

VII. ARGUMENTS (37 C.F.R. § 41.37(c)(1)(vii))

Based on the arguments and issues below, none of the claims stand or fall together, because in addition to having different scopes, each of the independent claims has a unique set of issues relating to its rejection and appeal as indicated in the arguments below:

Rejection of Claims 1-30 under 35 U.S.C. § 103(a)

In Section 7 of the Final Rejection, claims 1-30 were rejected under 35 U.S.C. § 103(a) as unpatentable over the DiNicola reference in view of the Ezer reference and further in view of the Herrera reference. For ease of reference, independent claims 1, 7, 14, 20, 26 and 27 are reproduced below:

1. (Previously Presented) Image processing circuitry, comprising:

a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space;

a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

7. (Previously Presented) For use in image processing circuitry that comprises a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating dual mode sub-processing circuitry that is associated with both of said pipelines, said method comprising:

determining whether said dual-mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode;

performing motion compensation operations associated with said two- dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said two-dimensional mode; and

performing rasterization operations associated said three-dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said three-dimensional mode.

14. (Previously Presented) Mode control circuitry for use in an image processing system having a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that processes two dimensional image data to generate successive two-dimensional image frames and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames, said mode control circuitry comprising:

dual mode sub-processing circuitry, associated with each of said two-dimensional and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof; and

a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in said two-dimensional mode and to perform said rasterization operations in said three-dimensional mode.

20. (Previously Presented) For use in image processing circuitry that comprises a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating mode control circuitry that is associated with both of said pipelines, said method comprising:

determining whether dual mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; and

controlling said dual mode sub-processing circuitry to perform either motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof in said two-dimensional mode, or rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof in said three-dimensional mode.

26. (Previously Presented) A media processing system having a central processing unit, a memory subsystem, an image processing system, and a display system, said media processing system comprising:

a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space of said display system;

a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space of said display system; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

27. (Previously Presented) Processing apparatus comprising:

a first specialty pipeline having a plurality of stages including a first stage and a last stage;

a second specialty pipeline having a plurality of stages including a first stage and a last stage; and

dual mode sub-processing circuitry operable in a selected one of first and second modes wherein in said first mode said dual-mode sub-processing circuitry forms an intermediate stage of said first specialty pipeline and in said second mode said dual-mode sub-processing circuitry forms an intermediate stage of said second specialty pipeline.

According to 35 U.S.C. § 103(a), "[a] patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art of such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains."

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing *a prima facie* case of obviousness. In re Fritch, 972 F.2d 1260,1262,23 U.S.P.Q. 2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny

patentability to a claimed invention is always upon the Patent Office. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, *9* F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim features. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. Id.

The Final Rejection asserts that the proposed multi-tiered combination of the DiNicola reference, the Ezer reference and the Herrera reference discloses or suggests the features of claims 1-30. In contrast with the assertions of the Final Rejection, the proposed combination of

the DiNicola, Ezer and Herrera references fails to disclose or suggest at least one feature of each of claims 1-30 and therefore fails to disclose or suggest each and every feature of claims 1-30.

A. Rejection of Claims 1-6

1) The Proposed Combination of the DiNicola, Ezer and Herrera References Fails to Disclose or Suggest Every Feature of Claim 1

Claim 1, from which claims 2-6 depend, recites the features of dual mode sub-processing circuitry, associated with each of a two-dimensional image pipeline and a three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

The Final Rejection asserts that the DiNicola, Ezer, and Herrera references, if combined as proposed, disclose these features of claim 1. Specifically, the Final Rejection asserts that the DiNicola reference discloses a 2D subsystem 301 that is purportedly analogous to the two-dimensional image pipeline of claim 1, a 3D processing node 305 that is purportedly analogous to the three-dimensional image pipeline of claim 1, and an attribute processor (AP) 306 that is purportedly analogous to the dual mode sub-processing circuitry of claim 1. Final Rejection, p. 4. The Final Rejection acknowledges that the DiNicola reference "is silent about [the features of] wherein when in said two-dimensional mode said dual-mode sub-processing circuitry performs operations associated with said two-dimensional image pipeline and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs operations

associated with said three-dimensional image pipeline" as recited by claim 1. Id. Accordingly, the Final Rejection relies on the teachings of the Ezer reference as allegedly disclosing

> a media coprocessor which supports 3-D graphics, video and audio. . . (col. 3, lines 1-26). The media processor 102 performs different operations using its several functional units such as :digital [sic] signal processor 202 that performs 2D and 3D functions (co., 4, lines 1-16) thus disclosing similarity in circuit implementation that allows common circuitry to share functions associated with two- and three-dimensional image pipelines and the seemingly different operation required thereby which is similarly recited in [claim 1].

Id.

The Final Rejection then concludes that "it would have been obvious to a person of ordinary skill in the art . . . to modify the '(attribute processor (AP) 306)' with the feature 'a media coprocessor that is able to provide an application spectrum . . .' as taught by Ezer et al because it results in improved cost/performance to applications." Id.

The Final Rejection also acknowledges that the DiNicola reference fails to disclose or suggest graphics operations associated with said two-dimensional image pipeline in one mode as recited by claim 1. See Id., p. 4. The Final Rejection therefore turns to the Herrera reference, which purportedly discloses "using a graphics engine to generate digital image data based on at least one command similar to 'one mode or another' as per [claim 1] and the same graphics engine generating motion compensated digital image data base on at least one digital image map and at least one motion vector (col. 5, lines 5-67; col. 6, lines 1-11)." Id., pp. 4-5. The Final Rejection therefore erroneously concludes that one of ordinary skill in the art would be motivated to modify the proposed combination of the DiNicola and Ezer references using the teachings of the Herrera reference "because it provides a cost-effective solution for doing both 2D ad 3D processing in one system (col. 6, lines 1-11; col. 13, lines 66-67; col. 14, lines 1-6)." Final Rejection, p. 5.

Contrary to the assertions of the Final Rejection, the proposed combination the DiNicola, Ezer and Herrera references does not disclose or suggest every feature of claim 1. As noted above, claim 1 recites the features of dual-mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry *performs motion compensation operations* associated with said two-dimensional image pipeline *at an intermediate stage thereof* and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs *rasterization operations* associated with said three-dimensional image pipeline *at an intermediate stage thereof.* The Final Rejection proposes the modification of the attribute processor 306 of the DiNicola reference based on the media coprocessor 102 of the Ezer reference to arrive at the dual mode sub-processing circuitry of claim 1. Id., p. 4. However, such a modification, if made, would still fail to disclose or suggest the claimed features of wherein the dual mode sub-processing circuit performs motion compensation operations associated with the two-dimensional image pipeline at an intermediate stage of the two-dimensional image line or performs rasterization operations associated with the three-dimensional pipeline at an intermediate stage of the three-dimensional pipeline. Instead, the DiNicola reference discloses that:

> An attribute processor (AP) 306 *performs preprocessing of the incoming 2D and 3D data streams (such as graphics attribute processing) and dispatches work to the 3D processing nodes 305 or to the 2D subsystem 301, as appropriate.* Attribute processor 306 may be either a suitably programmed general-purpose processor or a special-purpose logic circuit.
>
> Attribute processor 306 reads work from an input FIFO, memory or other input path and *moves work groups to the appropriate processing node 305.* This processor is also responsible for operations such as including a sequence number with the work groups so that the work groups may be reordered *after processing*

> *by the processing nodes 305*. Also, for some graphics data streams, the processor may perform display list processing and non-drawing processing.
>
> Attribute processor 306 is utilized to parse or partition the 3D data stream into multiple segments in accordance with a preferred embodiment of the present invention. Each segment is also called a work group (WG), and each work group may contain one or more work elements. The number of work elements in a work group may be determined by various factors such as the amount of processing time that it takes to process a work group versus the amount of processing time it takes to group work elements into a work group. Attribute processor 306 is coupled to a RAM 308, which is employed to store various instructions or data utilized by attribute processor 306. Additionally, attribute processor 306 may move data by utilizing other devices such as DMA controllers, processors, or with internal features within the attribute processor itself. Attribute processor 306 may perform graphics processing and supply current attribute data to the processing nodes 305 along with the work to be done.

The DiNicola Reference, col. 5, line 55 – col. 6, line 21 (emphasis added).

The above-cited passage provides that the attribute processor 306 "performs preprocessing of the incoming 2D and 3D data streams (such as graphics attribute processing)." See Id. One of ordinary skill in the art will appreciate that the *pre*processing of incoming 2D and 3D data streams by the attribute processor 306 as described by the DiNicola reference does not disclose, imply or suggest that the attribute processor 306 could be modified to perform motion compensation operations or rasterization operations in view of the teachings of the Ezer reference at least for the reason that these operations are core image processing operations and therefore do not fall into the "preprocessing" of incoming 2D and 3D data streams as the DiNicola reference ascribes to the attribute processor 306. Moreover, as discussed in detail below, the modification of the attribute processor 306 to perform actual image processing operations would destroy the parallel 2D/3D data stream processing goal to which the DiNicola reference aspires because the processing of each data stream would have to rely on the attribute processor 306 as a single, shared component, therefore preventing the 2D data stream and 3D

data stream from being processed *in parallel*, as well as introducing a delay in processing, which the DiNicola reference seeks to avoid.

Even if it is assumed, *arguendo*, that the attribute processor 306 could be so modified without destroying the functionality of the system of the DiNicola reference, such a modification would not result in the performance of motion compensation operations or rasterization operations at intermediate stages of the two- and three-dimensional image pipelines as provided by claim 1. There is no support for the modification of the attribute processor 306 to perform graphics operations at intermediate stages of the 2D graphics subsystem 301 or the 3D graphics nodes 305 as the DiNicola reference provides no disclosure or suggestion that any communications occur between elements 301, 305 and 306 at the intermediate stages nor does the DiNicola reference provide any disclosure enabling such communications. Instead, as disclosed by the DiNicola reference, the attribute processor 306 functions *prior to the initial stages* of the 2D subsystem 301 and 3D processing node 305 which the Examiner asserts are analogous to the two-dimensional and three-dimensional image processing pipelines, respectively, of claim 1, and therefore would not function *at intermediate stages* of the two- and three-dimensional image pipelines as provided by claim 1. The DiNicola reference therefore not only fails to disclose or suggest the features of performing motion compensation operations or rasterization operations at intermediate stages of the two- and three-dimensional image pipelines as provided by claim 1, the DiNicola reference teaches away from these features because it teaches that the attribute processor 306 operates prior to the 2D graphics subsystem 301 and the 3D graphics nodes 305.

Thus, as described above, none of the DiNicola, Ezer or Herrera references disclose or suggest, alone or in combination, at least the features of claim 1 of: dual mode sub-processing

circuitry, associated with each of a two-dimensional image pipeline and a three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode; wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof; and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof. The proposed combination of the DiNicola, Ezer and Herrera references therefore fails to disclose or suggest each and every feature of claim 1.

2) The Proposed Combination of the DiNicola, Ezer and Herrera References is Improper

Not only does the combination of the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 1, there is no motivation to combine the teachings of the DiNicola, Ezer and Herrera references as proposed by the Final Rejection. The Final Rejection provides merely general statements of motivation such as "improved cost/performance to applications" and "a cost-effective solution for doing both 2D and 3D processing in one system." See Final Rejection, p. 5. Vague allegations of improved cost and performance, without specifically describing how the proposed combination of teachings would achieve these goals, are insufficient demonstrations of motivation for one of ordinary skill in the art to combine the teachings. Moreover, the proposed combination of the DiNicola, Ezer and Herrera references is contrary to the teachings of the DiNicola, Ezer and Herrera references. As disclosed by the DiNicola reference:

> Systems which are currently on the market providing 2D and 3D data stream support *process these data streams sequentially, i.e., by time-multiplexing them on a single processor or processor complex.* They process one data stream for a period of time, then they process the second for a period of time, and then they return to the first. *This approach is an unacceptable solution since intermixing a data stream which is computationally intensive with one that is highly interactive generally degrades both.* The computationally intensive one (3D) does not get as much processor time as it might, and the interactive one (2D) must wait for the 3D data stream to be processed before getting an opportunity to display the interactive information that the user is waiting for. Currently available systems require large amounts of context information to be swapped in order to switch from processing 3D information to processing 2D information and back. . . . However, *the traditional approach of time-slicing between the two types of datastreams can cause serious performance problems*, as noted above."

The DiNicola Reference, col. 1, line 53 – col. 2, line 10 (emphasis added).

As demonstrated by the above-cited passage, the DiNicola reference teaches that the sequential processing (i.e., time-multiplexing) of a 2D data stream and a 3D data stream is "an unacceptable solution." To overcome this "unacceptable solution," the DiNicola reference teaches a system whereby a 2D data stream and a 3D data stream are "processed concurrently (i.e., in parallel) in such a manner that processing of the 2D data stream is not held up by processing of the 3D data stream." Id., Abstract. In contrast, the invention of the Ezer reference "relates to an integrated media coprocessing chip which partitions 3-D graphics, video, and audio tasks through time division multiplexing." The Ezer Reference, col. 2, lines 10-13; see also the Ezer Reference, col. 1, line 67-col. 2, line 2 ("With the media co-processor chip, the present invention partitions different media tasks so that they are performed sequentially in a time-division multiplexed format"). The Ezer reference teaches that the motivation for the sequential performance of different media tasks is to "provide a much less expensive computing system without sacrificing much in the way of functionality, quality and versatility. The present invention achieves this by designing a single, integrated media co-processor chip which is capable of processing graphics, video and audio. This reduced costs because it minimizes

duplicate functionalities and redundant circuitry." The Ezer Reference, col. 1, lines 62- 66. Thus, whereas the DiNicola reference seeks improved performance by adding additional, duplicative and redundant circuitry (and thereby increasing the complexity and cost) so that 2D and 3D data streams can be processed in parallel to improve performance, the Ezer reference teaches the reduction of additional, duplicative functionalities and redundant circuitry so as to reduce cost. As such, the approaches of the DiNicola reference and the Ezer reference are diametrically opposed and it therefore will be appreciated that the modification of the teachings of the DiNicola reference by the teachings of the Ezer reference to allegedly arrive at the features of claim 1 is contrary to both the improved performance/duplicative circuitry approach of the DiNicola reference and the reduced cost/reduced circuitry approach of the Ezer reference and therefore would destroy both of their respective advantages.[1] Accordingly, one of ordinary skill in the art, considering the teachings of DiNicola and Ezer in their entirety, would find no motivation to combine their teachings as proposed by the Final Rejection.

3) Claims 1-6 are Allowable under 35 U.S.C. § 103(a)

As described in sections 1 and 2 above, there is no motivation to combine the DiNicola, Ezer and Herrera references, and even if so combined, the DiNicola, Ezer and Herrera references

[1] The Advisory Action argues the position that the DiNicola and Ezer references are diametrically opposed is unpersuasive "for the reason that it highlights what each invention is incrementally striving [sic] and the argument is applied selectively." Advisory Action. The Advisory Action then continues by stating "DiNicola's invention processes two data stream[s] efficiently *without mutual interference* (col. 2, lines 5-10) and Ezer's media coprocessor chip does the same with *partitioned time-division multiplexed scheme* wherein certain circuits are used to perform the same functions with respect to audio, video and/or 3-D graphics applications (col. 2, lines 24-31)" Id. (emphasis added). As understood by one of ordinary skill in the art, the "partitioned time-division multiplexed scheme" of the Ezer reference *necessarily results in mutual interference* between the components participating the time-multiplexing scheme as one component must stall until its turn to use the shared component (i.e., must stall until the other component is done using the shared component for its allotted time) and vice versa. Introducing interference as such, the "partitioned time-division multiplexed scheme" of the Ezer reference is contrary and entirely inconsistent with processing of "two data stream[s] efficiently *without mutual interference*" taught by the DiNicola reference. Thus, rather than establishing that the combination of the DiNicola reference and the Ezer reference is proper, the Advisory Action affirms the Appellants' position of the improper combination of the DiNicola and Ezer references.

fail to disclose or suggest each and every feature of claim 1, and therefore also fail to disclose or suggest each and every feature of claims 2-6 at least by virtue of their dependency from claim 1. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claims 1-6 under 35 U.S.C. § 103(a). Claims 1-6 therefore are allowable under 35 U.S.C § 103(a).

B. Rejection of Claims 7-13

1) The Proposed Combination of the DiNicola, Ezer and Herrera References Fails to Disclose or Suggest Every Feature of Claim 7

Claim 7, from which claims 8-13 depend, recites a method of operating dual mode sub-processing circuitry that is associated with both of a two-dimensional image pipeline and a three-dimensional image pipeline, the method comprising: determining whether a dual-mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; performing motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said two-dimensional mode; and performing rasterization operations associated [with] said three-dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said three-dimensional mode.

The Final Rejection asserts that the DiNicola, Ezer, and Herrera references, if combined as proposed, disclose or suggest each and every feature of claim 7. The Final Rejection's reasoning for the rejection is on the same basis as described above with respect to claim 1. However, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that is associated with both a two-dimensional image pipeline and a three-dimensional pipeline in any manner, much less

dual-mode sub-processing circuitry that performs motion compensation operations associated with the two-dimensional image pipeline and rasterization operations associated with the three-dimensional image pipeline depending on mode. Moreover, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that performs motion compensation operations at an intermediate stage of a two-dimensional image pipeline or rasterization operations at an intermediate stage of a three-dimensional image pipeline. Accordingly, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, the claimed features of: determining whether a dual-mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; performing motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said two-dimensional mode; and performing rasterization operations associated said three-dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said three-dimensional mode as recited by claim 7. The proposed combination of DiNicola, Ezer and Herrera therefore fails to disclose or suggest each and every feature of claim 7.

2) The Proposed Combination of the DiNicola, Ezer and Herrera References is Improper

Not only does the combination of the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 7, as noted above, there is no motivation to combine the teachings of the DiNicola, Ezer and Herrera references as proposed by the Final Rejection.

3) Claims 7-13 are Allowable under 35 U.S.C. § 103(a)

As described in sections 1 and 2 above, there is no motivation to combine the DiNicola, Ezer and Herrera references, and even if so combined, the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 7, and therefore also fail to disclose or suggest each and every feature of claims 8-13 at least by virtue of their dependency from claim 7. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claims 7-13 under 35 U.S.C. § 103(a). Claims 7-13 therefore are allowable under 35 U.S.C § 103(a).

C. Rejection of Claims 14-19

1) The Proposed Combination of the DiNicola, Ezer and Herrera References Fails to Disclose or Suggest Every Feature of Claim 14

Claim 14, from which claims 15-19 depend, recites mode control circuitry comprising: dual mode sub-processing circuitry, associated with each of a two-dimensional and a three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof; and a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in said two-dimensional mode and to perform said rasterization operations in said three-dimensional mode.

The Final Rejection asserts that the DiNicola, Ezer, and Herrera references, if combined as proposed, disclose or suggest each and every feature of claim 14. The Final Rejection's reasoning for the rejection is on the same basis as described above with respect to claims 1 and 7. However, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that is associated with both a two-dimensional image pipeline and a three-dimensional pipeline in any manner, much less dual-mode sub-processing circuitry that performs motion compensation operations associated with the two-dimensional image pipeline and rasterization operations associated with the three-dimensional image pipeline depending on mode. Moreover, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that performs motion compensation operations at an intermediate stage of a two-dimensional image pipeline or rasterization operations at an intermediate stage of a three-dimensional image pipeline. Accordingly, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, the features of: dual mode sub-processing circuitry, associated with each of a two-dimensional and a three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof; and a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in said two-dimensional mode and to perform said rasterization operations in said three-dimensional mode as recited by

claim 14. The proposed combination of DiNicola, Ezer and Herrera therefore fails to disclose or suggest each and every feature of claim 14.

2) The Proposed Combination of the DiNicola, Ezer and Herrera References is Improper

Not only does the combination of the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 14, as noted above, there is no motivation to combine the teachings of the DiNicola, Ezer and Herrera references as proposed by the Final Rejection.

3) Claims 14-19 are Allowable under 35 U.S.C. § 103(a)

As described in sections 1 and 2 above, there is no motivation to combine the DiNicola, Ezer and Herrera references, and even if so combined, the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 14, and therefore also fail to disclose or suggest each and every feature of claims 15-19 at least by virtue of their dependency from claim 14. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claims 14-19 under 35 U.S.C. § 103(a). Claims 14-19 therefore are allowable under 35 U.S.C § 103(a).

D. Rejection of Claims 20-25

1) The Proposed Combination of the DiNicola, Ezer and Herrera References Fails to Disclose or Suggest Every Feature of Claim 20

Claim 20, from which claims 21-25 depend, recites a method of operating dual mode sub-processing circuitry that is associated with both of a two-dimensional image pipeline and a three-dimensional image pipeline, the method comprising: determining whether dual mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; and controlling

said dual mode sub-processing circuitry to perform either motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof in said two-dimensional mode, or rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof in said three-dimensional mode.

The Final Rejection asserts that the DiNicola, Ezer, and Herrera references, if combined as proposed, disclose or suggest each and every feature of claim 20. The Final Rejection's reasoning for the rejection is on the same basis as described above with respect to claims 1, 7 and 14. However, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that is associated with both a two-dimensional image pipeline and a three-dimensional pipeline in any manner, much less dual-mode sub-processing circuitry that performs motion compensation operations associated with the two-dimensional image pipeline and rasterization operations associated with the three-dimensional image pipeline depending on mode. Moreover, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that performs motion compensation operations at an intermediate stage of a two-dimensional image pipeline or rasterization operations at an intermediate stage of a three-dimensional image pipeline. Accordingly, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, the features of: determining whether dual mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; and controlling said dual mode sub-processing circuitry to perform either motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof in said two-dimensional mode, or rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof in said three-dimensional mode as recited by

claim 20. The proposed combination of DiNicola, Ezer and Herrera therefore fails to disclose or suggest each and every feature of claim 20.

2) The Proposed Combination of the DiNicola, Ezer and Herrera References is Improper

Not only does the combination of the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 20, as noted above, there is no motivation to combine the teachings of the DiNicola, Ezer and Herrera references as proposed by the Final Rejection.

3) Claims 20-25 are Allowable under 35 U.S.C. § 103(a)

As described in sections 1 and 2 above, there is no motivation to combine the DiNicola, Ezer and Herrera references, and even if so combined, the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 20, and therefore also fail to disclose or suggest each and every feature of claims 20-25 at least by virtue of their dependency from claim 20. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claims 20-25 under 35 U.S.C. § 103(a). Claims 20-25 therefore are allowable under 35 U.S.C § 103(a).

E. Rejection of Claim 26

1) The Proposed Combination of the DiNicola, Ezer and Herrera References Fails to Disclose or Suggest Every Feature of Claim 26

Claim 26 recites the features of dual mode sub-processing circuitry, associated with each of a two-dimensional image pipeline and a three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation

operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

The Final Rejection asserts that the DiNicola, Ezer, and Herrera references, if combined as proposed, disclose or suggest each and every feature of claim 26. The Final Rejection's reasoning for the rejection is on the same basis as described above with respect to claims 1, 7, 14 and 20. However, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that is associated with both a two-dimensional image pipeline and a three-dimensional pipeline in any manner, much less dual-mode sub-processing circuitry that performs motion compensation operations associated with the two-dimensional image pipeline and rasterization operations associated with the three-dimensional image pipeline depending on mode. Moreover, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that performs motion compensation operations at an intermediate stage of a two-dimensional image pipeline or rasterization operations at an intermediate stage of a three-dimensional image pipeline. Accordingly, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, the features of: dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-

dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof as recited by claim 26. The proposed combination of DiNicola, Ezer and Herrera therefore fails to disclose or suggest each and every feature of claim 26.

2) The Proposed Combination of the DiNicola, Ezer and Herrera References is Improper

Not only does the combination of the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 26, as noted above, there is no motivation to combine the teachings of the DiNicola, Ezer and Herrera references as proposed by the Final Rejection.

3) Claims 26 are Allowable under 35 U.S.C. § 103(a)

As described in sections 1 and 2 above, there is no motivation to combine the DiNicola, Ezer and Herrera references, and even if so combined, the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 26. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claims 26 under 35 U.S.C. § 103(a). Claim 26 therefore is allowable under 35 U.S.C § 103(a).

F. Rejection of Claims 27-30

1) The Proposed Combination of the DiNicola, Ezer and Herrera References Fails to Disclose or Suggest Every Feature of Claim 27

Claim 27, from which claims 28-30 depend, recites the features of dual mode sub-processing circuitry operable in a selected one of first and second modes wherein in said first mode said dual-mode sub-processing circuitry forms an intermediate stage of a first specialty

pipeline and in said second mode said dual-mode sub-processing circuitry forms an intermediate stage of a second specialty pipeline.

The Final Rejection asserts that the DiNicola, Ezer, and Herrera references, if combined as proposed, disclose or suggest each and every feature of claim 27. The Final Rejection's reasoning for the rejection is on the same basis as described above with respect to claims 1, 7, 14, 20 and 26. However, as similarly described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that is associated with two specialty pipelines in any manner. Moreover, as described above, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, dual-mode sub-processing circuitry that forms intermediate stages of two specialty pipelines. Accordingly, the DiNicola, Ezer and Herrera references fail to disclose or suggest, alone or in combination, the features of: dual mode sub-processing circuitry operable in a selected one of first and second modes wherein in said first mode said dual-mode sub-processing circuitry forms an intermediate stage of a first specialty pipeline and in said second mode said dual-mode sub-processing circuitry forms an intermediate stage of a second specialty pipeline as recited by claim 27. The proposed combination of DiNicola, Ezer and Herrera therefore fails to disclose or suggest each and every feature of claim 27.

2) The Proposed Combination of the DiNicola, Ezer and Herrera References is Improper

Not only does the combination of the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 27, as noted above, there is no motivation to combine the teachings of the DiNicola, Ezer and Herrera references as proposed by the Final Rejection.

3) Claims 27-30 are Allowable under 35 U.S.C. § 103(a)

As described in sections 1 and 2 above, there is no motivation to combine the DiNicola, Ezer and Herrera references, and even if so combined, the DiNicola, Ezer and Herrera references fail to disclose or suggest each and every feature of claim 27, and therefore also fail to disclose or suggest each and every feature of claims 28-35 at least by virtue of their dependency from claim 27. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claims 20-25 under 35 U.S.C. § 103(a). Claims 20-25 therefore are allowable under 35 U.S.C § 103(a).

G. Rejection of Claims 3 and 9

1) The Proposed Combination of the DiNicola, Ezer and Herrera References Fails to Disclose or Suggest Every Feature of Claims 3 and 9

Claims 3, which depends from claim 1, recites the additional features of wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said two-dimensional mode and to blend samples from a plurality of texture maps in said three-dimensional mode. Claim 9, which depends from claim 7, recites related additional features of blending one of samples from a plurality of reference frames in said two-dimensional mode and samples from a plurality of texture maps in said three-dimensional mode.

The Final Rejection cites col. 11, lines 1-22 of the Ezer reference as disclosing these features. See Final Rejection, p. 6. For ease of reference, this cited passage is reproduced below:

> The image display can be optimized with 2D texture coordinates without perspective correction, planar source data (without mipmap [sic] level-of-detail trilinear interpolations), and YUV texture values for video. Furthermore, sprites can be optimized by reusing data in on-chip texture memory and point sampling. The MDP also performs the spatial domain portion of video decompression, such as motion compensation and reconstruction. *In addition, MDP 805 performs image scaling, filtering, keying, and compositing functions for MPEG video. For 3D graphics, MDP 805 performs rasterization, texture resampling, shading, color combination, blending, and Z buffering functions.* Because the MDP is limited to display precision, it can be implemented with 8-bit multipliers, whereas the more general audio and video processing applications of the MSP require 16bit multipliers. While the media coprocessor performs many application functions, at any particular time, the entire media coprocessor is performing one function, such as MPEG or 3-D graphics. Over a given time interval (e.g., a frame time), the media coprocessor switches between the various functions, but at a coarse granularity, such as generating a frame of 3-D graphics or a frame of MPEG video.

The Ezer Reference, col. 11, lines 1-22 (emphasis added).

The relied-upon passage of the Ezer reference merely provides that the MDP 805 can perform, "for 3D graphics, rasterization, texture resampling, shading, color combination, blending and Z buffering functions." Id. Although this passage discloses that the MDP 805 performs "blending," the Ezer reference does not disclose or suggest that the blending performed by the MDP 805 involves blending samples from a plurality of reference frames or blending samples from a plurality of texture maps. Moreover, the relied-upon passage provides that the "blending" is "for 3D graphics" and fails to disclose or suggest blending of any kind for 2D graphics. Accordingly, the proposed combination of the DiNicola and Ezer references fails to disclose or suggest the claimed features of: wherein a portion of said dual mode sub-processing circuitry is further operable to blend *samples from a plurality of reference frames in said two-dimensional mode* and to blend samples *from a plurality of texture maps* in said three-dimensional mode as recited by claim 3. Similarly, the proposed combination of the DiNicola and Ezer references fails to disclose or suggest the claimed features of: blending one of *samples*

from a plurality of reference frames in said two-dimensional mode and samples *from a plurality of texture maps* in said three-dimensional mode as recited by claim 9.

2) Claims 3 and 9 are Allowable under 35 U.S.C. § 103(a)

As described above, there is no motivation to combine the DiNicola and Ezer references, and even if so combined, the DiNicola and Ezer references fail to disclose or suggest each and every feature of claims 3 and 9. Accordingly, the Final Rejection fails to establish a *prima facie* case of obviousness in support of its rejection of claims 3 and 9 under 35 U.S.C. § 103(a). Claims 3 and 9 therefore are allowable under 35 U.S.C § 103(a).

VIII. CONCLUSION

For at least the reasons given above, all pending claims are allowable and the Appellants therefore respectfully request reconsideration and allowance of all claims and that this patent application be passed to issue.

Respectfully submitted,

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Date

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IX. APPENDIX OF CLAIMS INVOLVED IN THE APPEAL (37 C.F.R. § 41.37(c)(1)(viii))

The text of each claim involved in the appeal is as follows:

1. (Previously Presented) Image processing circuitry, comprising:

a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space;

a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

2. (Previously Presented) The image processing circuitry set forth in Claim 1 wherein a portion of said dual mode sub-processing circuitry is further operable to sample reference frames in said two-dimensional mode and to perform texture mapping in said three-dimensional mode.

3. (Previously Presented) The image processing circuitry set forth in Claim 1 wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said two-dimensional mode and to blend samples from a plurality of texture maps in said three-dimensional mode.

4. (Previously Presented) The image processing circuitry set forth in Claim 2 wherein a portion of said dual mode sub-processing circuitry is further operable to process said plurality of reference frames using error terms in said two-dimensional mode and to perform alpha blending in said three-dimensional mode.

5. (Previously Presented) The image processing circuitry set forth in Claim 1 wherein the image processing circuitry is operable to support at least one MPEG standard.

6. (Original) The image processing circuitry set forth in Claim 1 further comprising an alpha blend sub-circuitry that is operable to process at least 8- and 9-bit signed values.

7. (Previously Presented) For use in image processing circuitry that comprises a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating dual mode sub-processing circuitry that is associated with both of said pipelines, said method comprising:

determining whether said dual-mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode;

performing motion compensation operations associated with said two- dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said two-dimensional mode; and

performing rasterization operations associated said three-dimensional image pipeline at an intermediate stage thereof using said dual-mode sub-processing circuitry in said three-dimensional mode.

8. (Previously Presented) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising:

sampling a plurality of reference frames in said two-dimensional mode; and

performing texture mapping in said three-dimensional mode.

9. (Previously Presented) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising blending one of samples from a plurality of reference frames in said two-dimensional mode and samples from a plurality of texture maps in said three-dimensional mode.

10. (Previously Presented) The method of operating said dual mode sub-processing circuitry set forth in Claim 8 further comprising:

processing said plurality of reference frames using error terms in said two-dimensional mode; and

performing alpha blending in said three-dimensional mode.

11. (Previously Presented) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising switching from said three-dimensional mode to said two-dimensional mode to perform motion compensation in accordance with at least one MPEG standard.

12. (Previously Presented) The method of operating said dual mode sub-processing circuitry set forth in Claim 10 wherein performing alpha blending further comprises processing at least 8- and 9-bit signed values.

13. (Previously Presented) The method of operating said dual mode sub-processing circuitry set forth in Claim 7 further comprising controlling said dual mode sub-processing circuitry.

14. (Previously Presented) Mode control circuitry for use in an image processing system having a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that processes two dimensional image data to generate successive two-dimensional image frames and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames, said mode control circuitry comprising:

dual mode sub-processing circuitry, associated with each of said two-dimensional and said three-dimensional image pipelines, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof; and

a controller that is operable to control said dual mode sub-processing circuitry to perform said motion compensation operations in said two-dimensional mode and to perform said rasterization operations in said three-dimensional mode.

15. (Previously Presented) The mode control circuitry set forth in Claim 14 wherein a portion of said dual mode sub-processing circuitry is further operable to sample a plurality of reference frames in said two-dimensional mode and to perform texture mapping in said three-dimensional mode.

16. (Previously Presented) The mode control circuitry set forth in Claim 14 wherein a portion of said dual mode sub-processing circuitry is further operable to blend samples from a plurality of reference frames in said two-dimensional mode and to blend samples from a plurality of texture maps in said three-dimensional mode.

17. (Previously Presented) The mode control circuitry set forth in Claim 15 wherein a portion of said dual mode sub-processing circuitry is further operable to process said plurality of reference frames using error terms in said two-dimensional mode and to perform alpha blending in said three-dimensional mode.

18. (Original) The mode control circuitry set forth in Claim 14 wherein said dual mode sub-processing circuitry is operable to support at least one MPEG standard.

19. (Original) The mode control circuitry set forth in Claim 14 further comprising an alpha blend sub-circuitry that is operable to process at least 8-bit and 9-bit signed values.

20. (Previously Presented) For use in image processing circuitry that comprises a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage and a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage, said two-dimensional image pipeline operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space, and said three-dimensional image pipeline operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space, a method of operating mode control circuitry that is associated with both of said pipelines, said method comprising:

determining whether dual mode sub-processing circuitry is in a two-dimensional mode or a three-dimensional mode; and

controlling said dual mode sub-processing circuitry to perform either motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof in said two-dimensional mode, or rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof in said three-dimensional mode.

21. (Previously Presented) The method of operating said mode control circuitry set forth in Claim 20 further comprising:

sampling a plurality of reference frames in said two-dimensional mode; and

performing texture mapping in said three-dimensional mode.

22. (Previously Presented) The method of said operating mode control circuitry set forth in Claim 20 further comprising:

blending samples from a plurality of reference frames in said one two-dimensional mode; and

blending samples from a plurality of texture maps in said other three-dimensional mode.

23. (Previously Presented) The method of operating said mode control circuitry set forth in Claim 21 further comprising:

processing said plurality of reference frames using error terms in said one two-dimensional mode; and

performing alpha blending in said three-dimensional mode.

24. (Previously Presented) The method of operating said mode control circuitry set forth in Claim 20 wherein said dual mode sub-processing circuitry is operable to support at least one MPEG standard.

25. (Previously Presented) The method of operating mode control circuitry set forth in Claim 20 further comprising controlling said dual-mode sub-processing circuitry using an alpha blend sub-circuitry that is operable to process at least 8-bit and 9- bit signed values.

26. (Previously Presented) A media processing system having a central processing unit, a memory subsystem, an image processing system, and a display system, said media processing system comprising:

a two-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space of said display system;

a three-dimensional image pipeline having a plurality of stages including a first stage and a last stage that is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space of said display system; and

dual mode sub-processing circuitry, associated with each of said two-dimensional image pipeline and said three-dimensional image pipeline, that is operable in a selected one of a two-dimensional mode and a three-dimensional mode, wherein when in said two-dimensional mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline at an intermediate stage thereof and wherein when in said three-dimensional mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline at an intermediate stage thereof.

27. (Previously Presented) Processing apparatus comprising:

a first specialty pipeline having a plurality of stages including a first stage and a last stage;

a second specialty pipeline having a plurality of stages including a first stage and a last stage; and

dual mode sub-processing circuitry operable in a selected one of first and second modes wherein in said first mode said dual-mode sub-processing circuitry forms an intermediate stage of said first specialty pipeline and in said second mode said dual-mode sub-processing circuitry forms an intermediate stage of said second specialty pipeline.

28. (Previously Presented) The processing apparatus of claim 27 wherein said first specialty pipeline comprises a two-dimensional image pipeline that is operable to process two dimensional image data to generate successive two-dimensional image frames for display in a two-dimensional image space of a display system.

29. (Previously Presented) The processing apparatus of claim 28 wherein said second specialty pipeline is operable to process three-dimensional image data to render successive three-dimensional image frames for display in a two-dimensional image space of said display system.

30. (Previously Presented) The processing apparatus of claim 29 wherein when in said first mode said dual mode sub-processing circuitry performs motion compensation operations associated with said two-dimensional image pipeline and when in said second mode said dual mode sub-processing circuitry performs rasterization operations associated with said three-dimensional image pipeline.